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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/802,203

03/17/2004

Roy J. Blazek

34282

3763

7590

02/22/2006

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EXAMINER

GREEN, PHILLIP

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/802,203

Applicant(s)

BLAZEK ET AL.

Examiner

Phillip S. Green

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 6/21/04
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Information Disclosure Statement*

1. The information disclosure statement (IDS) submitted on 06/21/2004 was filed after the mailing date of the application. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Setzer et al. (US 2003/0015277 A1) in view of Naumov et al. (US 6,875, 950 B2).

Re claim 1, Setzer discloses a method of creating a monolithic circuit structure, the method comprising the steps of:

- placing a circuit component onto an individual layer of substrate;
- firing the individual layer of substrate and the circuit component placed thereon;
- applying a bonding agent to the individual layer of substrate and assembling the individual layer of substrate with one or more other layers of substrate; and
- firing the assembled individual layer of substrate and one or more other layers of substrate together to activate the bonding agent, thereby bonding the individual layer of

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substrate to the one or more other layers of substrate and creating the monolithic circuit structure. (Note: Para 0002-0004).

However, Setzer does not explicitly disclose adjusting the circuit component as necessary to achieve a desired degree of precision.

Naumov discloses the laser trimming of passive circuit elements such as resistors, capacitors and inductors. (Note: Abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to use the laser trimming taught by Naumov in the invention of Setzer in order to achieve narrow final resistor tolerances. (Note: Naumov; Col. 10, line 5-9).

Re claim 2, Setzer and Naumov discloses all the claimed limitation according to Claim 1 in the paragraph above, including, wherein the circuit component is selected from the group consisting of: resistors, capacitors, and inductors. (Note: Naumov; Col 4, lines 1 – 14).

Re claim 3, Setzer and Naumov discloses all the claimed limitation according to Claim 1 in the paragraph above, including, wherein the circuit component is placed onto the individual layer of substrate by screen-printing. (Note: Naumov; Col 6, lines 39 –51).

Re claim 4, Setzer and Naumov discloses all the claimed limitation according to Claim 1 in the paragraph above, including, wherein the individual layer of substrate and the one or more other layers of substrate are pre-fired thick film ceramic substrate. (Note: Naumov; Col 8, lines 1-3).

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Re claim 5, Setzer and Naumov discloses all the claimed limitation according to Claim 1 in the paragraph above, including, wherein the individual layer of substrate and the one or more other layers of substrate are standard alumina thick film ceramic substrates. (Note: Naumov; Col 8, lines 1-3).

Re claim 6, Setzer and Naumov discloses all the claimed limitation according to Claim 1 in the paragraph above, including, wherein the bonding agent is a thick film glass. (Note: Naumov; Col 8, lines 34 – 37; Col 9, lines 8 - 13).

Re claim 7, Setzer discloses a method of creating a multi-layered monolithic circuit structure, the method comprising the steps of:

printing a circuit component onto an individual layer of thick film ceramic substrate;

firing the individual layer of thick film ceramic substrate and the circuit component printed thereon;

applying a bonding agent to the individual layer of thick film ceramic substrate and assembling the individual layer of thick film ceramic substrate with one or more other layers of thick film ceramic substrate; and

firing the assembled individual layer of thick film ceramic substrate and one or more other layers of thick film ceramic substrate together to activate the bonding agent, thereby bonding the individual layer of thick film ceramic substrate to the one or more other layers of thick film ceramic substrate and creating the multi- layered monolithic circuit structure. (Note: Para 0002-0004).

However, Setzer does not explicitly disclose trimming the circuit component as necessary to achieve a desired degree of precision;

Naumov discloses the laser trimming of passive circuit elements such as resistors, capacitors and inductors. (Note: Abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to use the laser trimming taught by Naumov in the invention of Setzer in order to achieve narrow final resistor tolerances. (Note: Naumov; Col. 10, line 5-9).

Re claim 8, Setzer and Naumov discloses all the claimed limitation according to Claim 7 in the paragraph above, wherein the plurality of circuit components are selected from the group consisting of: resistors, capacitors, and inductors. (Note: Naumov; Col 4, lines 1 – 14).

Re claim 9, Setzer and Naumov discloses all the claimed limitation according to Claim 7 in the paragraph above, wherein the individual layers of thick film ceramic substrate are standard alumina thick film ceramic substrate. (Note: Naumov; Col 8, lines 1-3).

Re claim 10, Setzer and Naumov discloses all the claimed limitation according to Claim 7 in the paragraph above, wherein the bonding agent is a thick film glass. (Note: Naumov; Col 8, lines 34 – 37; Col 9, lines 8 - 13).

Re claim 11, Setzer and Naumov discloses a method of creating a multi-layered monolithic circuit structure, the method comprising the steps of:

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screen-printing a plurality of circuit components onto a plurality of individual layers of thick film ceramic substrate;

firing the individual layers of thick film ceramic substrate and the circuit components screen-printed thereon;

applying a thick film glass bonding agent to the individual layers of thick film ceramic substrate and assembling the individual layers of thick film ceramic substrate; and

firing the assembled individual layers of thick film ceramic substrate to sinter the thick film glass bonding agent, thereby bonding the individual layers of thick film ceramic substrate together and creating the multi-layered monolithic circuit structure. (Note: Para 0002-0004).

However, Setzer does not explicitly disclose trimming the circuit component as necessary to achieve a desired degree of precision;

Naumov discloses the laser trimming of passive circuit elements such as resistors, capacitors and inductors. (Note: Abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to use the laser trimming taught by Naumov in the invention of Setzer in order to achieve narrow final resistor tolerances. (Note: Naumov; Col. 10, line 5-9).

Re claim 12, Setzer and Naumov discloses all the claimed limitation according to Claim 11 in the paragraph above, wherein the plurality of circuit components are

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selected from the group consisting of: resistors, capacitors, and inductors. (Note: Col 4, lines 1 – 14).

Re claim 13, Setzer and Naumov discloses all the claimed limitation according to Claim 11 in the paragraph above, wherein the individual layers of thick film ceramic substrate are standard alumina thick film ceramic substrate. (Note: Naumov; Col 8, lines 1-3).

Re claim 14, Setzer and Naumov discloses a method of creating a multi-layered monolithic circuit structure, the method comprising the steps of:

screen-printing a plurality of circuit components onto a plurality of individual layers of substrate, wherein the circuit components are selected from the group consisting of: resistors, capacitors, and inductors, and wherein the individual layers of substrate are standard alumina thick film ceramic substrate;

firing the individual layers of substrate and the circuit components screen-printed thereon;

applying a thick film glass bonding agent to the individual layers of substrate and assembling the individual layers of substrate; and

firing the assembled individual layers of substrate to sinter the thick film glass bonding agent, thereby bonding the individual layers of substrate together and creating the multi-layered monolithic circuit structure. (Note: Para 0002-0004).

However, Setzer does not explicitly disclose trimming the circuit component as necessary to achieve a desired degree of precision;

Naumov discloses the laser trimming of passive circuit elements such as resistors, capacitors and inductors. (Note: Abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to use the laser trimming taught by Naumov in the invention of Setzer in order to achieve narrow final resistor tolerances. (Note: Naumov; Col. 10, line 5-9).

### ***Correspondence***

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip S. Green whose telephone number is 571-272-7024. The examiner can normally be reached on Monday thru Thursday 8:30 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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02/09/2006

  
**BROOK KEBEDE**  
**PRIMARY EXAMINER**